REMARKS

The application has been reviewed in light of the Office Action dated December 9, 2003. Claims 1-14 are pending, with claims 1 and 8 being in independent form. By this Amendment, Applicant has amended claims 1 and 8 to place the claim in better form for examination, by removing an informality, and to clarify the claimed invention.

The specification was objected to under 37 C.F.R. §1.75(d)(1) as purportedly failing to provide proper antecedent basis for the claimed subject matter.

The Office Action contends that the specification fails to provide proper antecedent basis for "a clock signal control part" and "said clock signal control part comprises a forward circuit part and a clock control part".

Applicant respectfully directs the Examiner's attention to the application at, for example, page 13, lines 8-10.

Accordingly, withdrawal of the objection to the specification is respectfully requested.

The drawings were objected to under 37 C.F.R. §1.83(a) as purportedly failing to show every feature of the invention specified in the claims.

Attached hereto as **Exhibit A** is a proposed drawing change to FIG. 1, to show a clock signal control part 9. Support for the drawing change can be found in the specification at, inter alia, page 13, lines 8-10.

Approval of the drawing change is respectfully requested.

Claim 8 was objected to as having an informality.

Claim 8 has been amended hereinabove to remove the obvious

typographical error.

Accordingly, withdrawal of the objection is respectfully requested.

Claims 1-7 were rejected under 35 U.S.C. §102(b) as purportedly anticipated by U.S. Patent No. 5,638,530 to Pawate. Claims 8-14 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Japanese Patent Application No. JP01264034A to Nakajima et al in view of Pawate.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1 and 8 are patentable over the cited art, for at least the following reasons.

This application relates to digital signal processors (DSPs) which have an internal memory for storing a program to be executed, such as for a modem. As discussed in the application at pages 1-2, recent developments in digital signal processing technology has been accompanied by more complex signal processing, which typically is associated with need for more program memory capacity. Although some conventional DSPs have an internal program memory, such DSP internal memories are limited in capacity. Therefore, programs required for the signal processing generally are stored on an external memory (such as a ROM) and when needed, transferred to the internal memory of the DSP. Since replacement of the program to be executed in the DSP internal memory must be performed on the fly (for example, during modem communication), conventional program replacement approaches which utilize a reset signal have a disadvantage that the reset incurs a great overhead for restarting program execution. Accordingly, there has been an unsatisfied need, in DSPs which have an internal memory,

for improved program replacement techniques which have a minimal overhead.

According to the present application, the disadvantages of conventional program replacement techniques are avoided by controlling a clock signal supplied to the internal memory of the DSP during program replacement, without requiring reinitialization of the digital signal processor.

For example, independent claim 1 is directed to a signal processing apparatus which includes a digital signal processor, an external memory part, a clock signal generating part and a clock signal control part. The digital signal processor includes an internal memory part which stores a program to be executed. The external memory part stores programs executable in the digital signal processor. The clock signal generating part generates a clock signal and outputs the clock signal to the digital signal processor. The clock signal control part controls output of the clock signal to the digital signal processor so that one or more of the programs stored in the external memory part can be forwarded to, and replace the program to be executed in, the internal memory part. Claim 1 has been amended to clarify that the control of output of the clock signal is performed without requiring reinitialization of the digital signal processor.

Pawate, as understood by Applicant, is directed to a smart card for improved speech, image and/or signal processing. The smart card acts as an interface between a host computer (containing, for example, application software) and an analog front end (AFE) which can be coupled to a fax or modem, a microphone a speaker, etc. The smart card includes a DSP (digital signal processor) onboard and a shared memory

which is external to the DSP and can be accessed by the host computer as well as by the DSP. In addition, the DSP has its own memory into which a program to be executed by the DSP is loaded. In a smart mode, the host computer can control the DSP by controlling the program stored in the memory of the DSP. However, according to Pawate, in order for the host computer to switch into the smart mode to control the DSP, the host computer must first load reset and interrupt vectors of the DSP (see Pawate, column 13, lines 59-61, column 14, lines 35-46). Only after the DSP has thus been initialized can the host computer then control the clock of the DSP.

Applicant does not find teaching or suggestion in Pawate, however, that the control of output of the clock signal is performed without requiring reinitialization of the digital signal processor.

Nakajima, as understood by Applicant, is directed to a digital signal processor built in a modem.

Applicant does not find disclosure or suggestion by the cited art, however, of a signal processing apparatus which includes a digital signal processor, an external memory part, a clock signal generating part and a clock signal control part, wherein the digital signal processor includes an internal memory part which stores a program to be executed, the clock signal control part controls output of the clock signal to the digital signal processor so that one or more of the programs stored in the external memory part can be forwarded to the internal memory part, and the control of output of the clock signal is performed without requiring reinitialization of the digital signal processor, as provided by independent claim 1 as amended.

Since the cited art does not disclose or suggest each and every

feature of the claimed invention, the cited art does not render the claimed invention unpatentable.

Independent claim 8 is patentably distinct from the cited art for at least similar reasons.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1 and 8, and the claims depending therefrom, are patentable over the cited references.

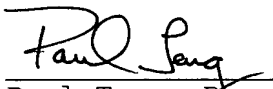
If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

The Office is hereby authorized to charge any additional fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,



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